Energy Efficient I3C IP Subsystem for Low Power IoT

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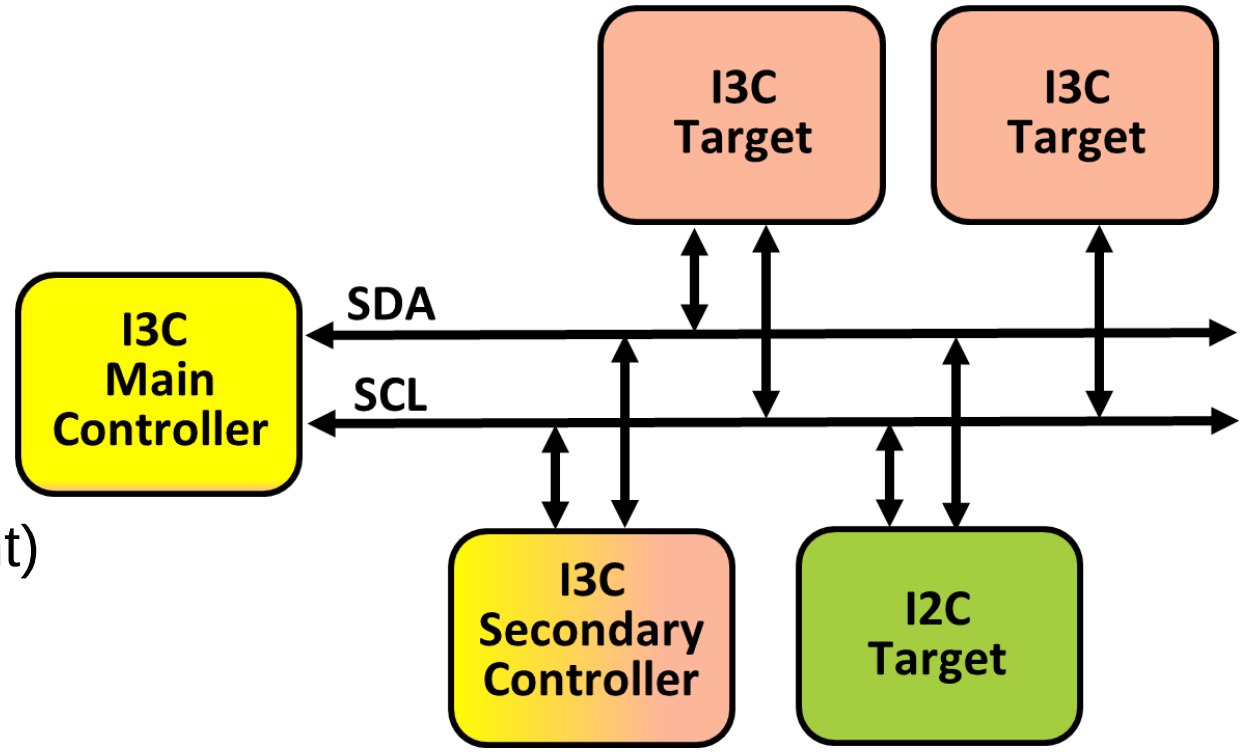
The I3C Interface

A powerful bidirectional two-wire interface for low power & space efficient design

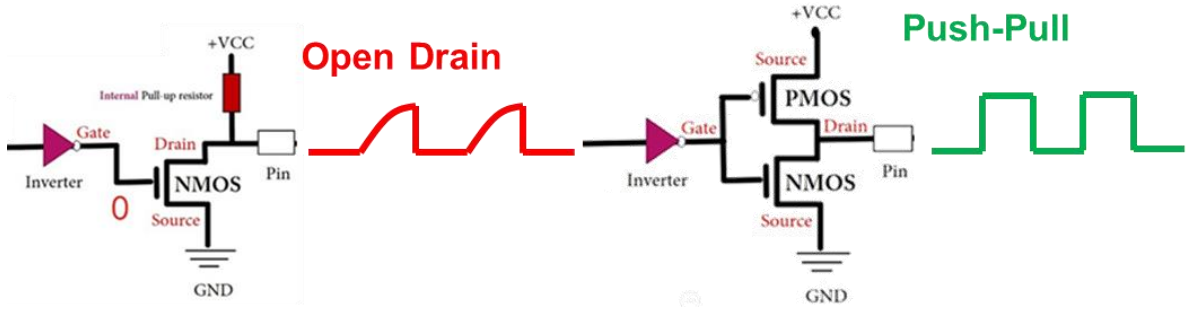
- **2-Wire** Powerful **Bidirectional**
- Backward **Compatibility**
- **Faster** Data Rates **(DDR/TSP/TSL)**
- **Dynamic** Addressing
- **Power Efficiency**
- **Advanced Features (IBI/HJ)**
- **In-Band** Interrupt (**reduced p**in count)
- Multi-drop capability

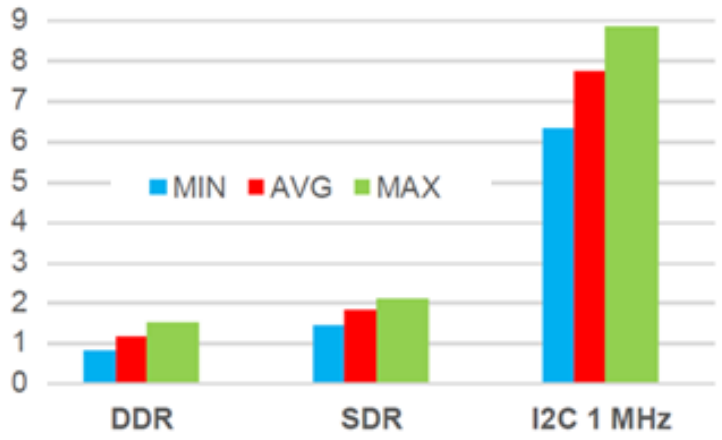


I3C Bus- Low Energy & Power Features

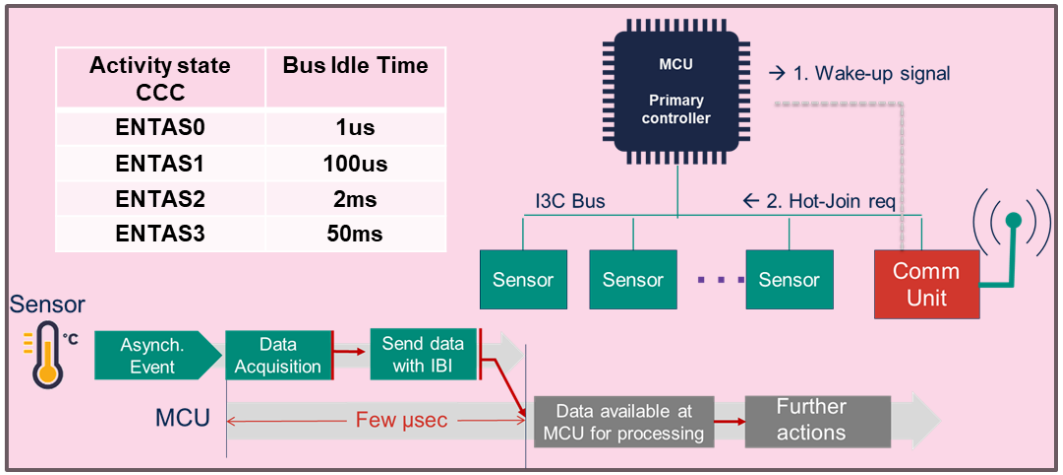
I3C Power efficiency

- Push-Pull vs. Open-Drain
- Faster DATA Rates
- Built-in Power Management
- In-Band Interrupts
- Reduced Communication



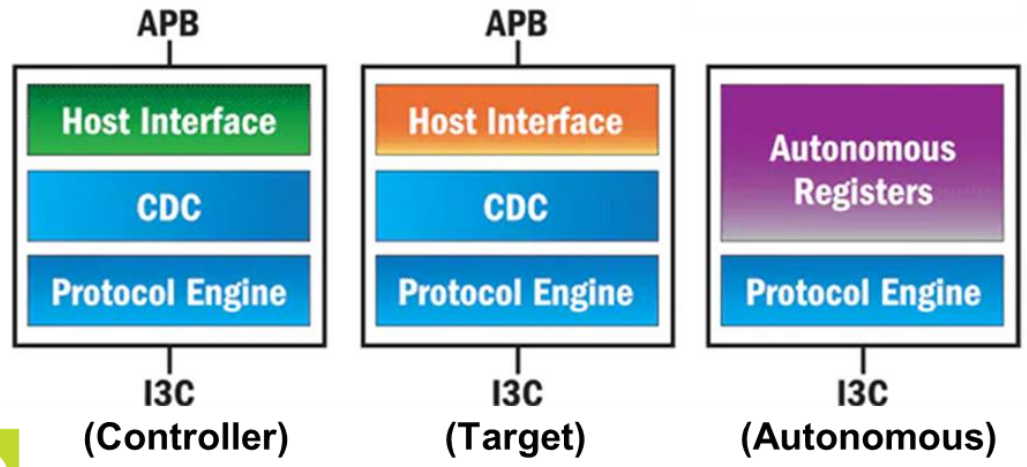


I3C vs. I²C FM+ Energy per 1 kB Effective Data Block, in µJ

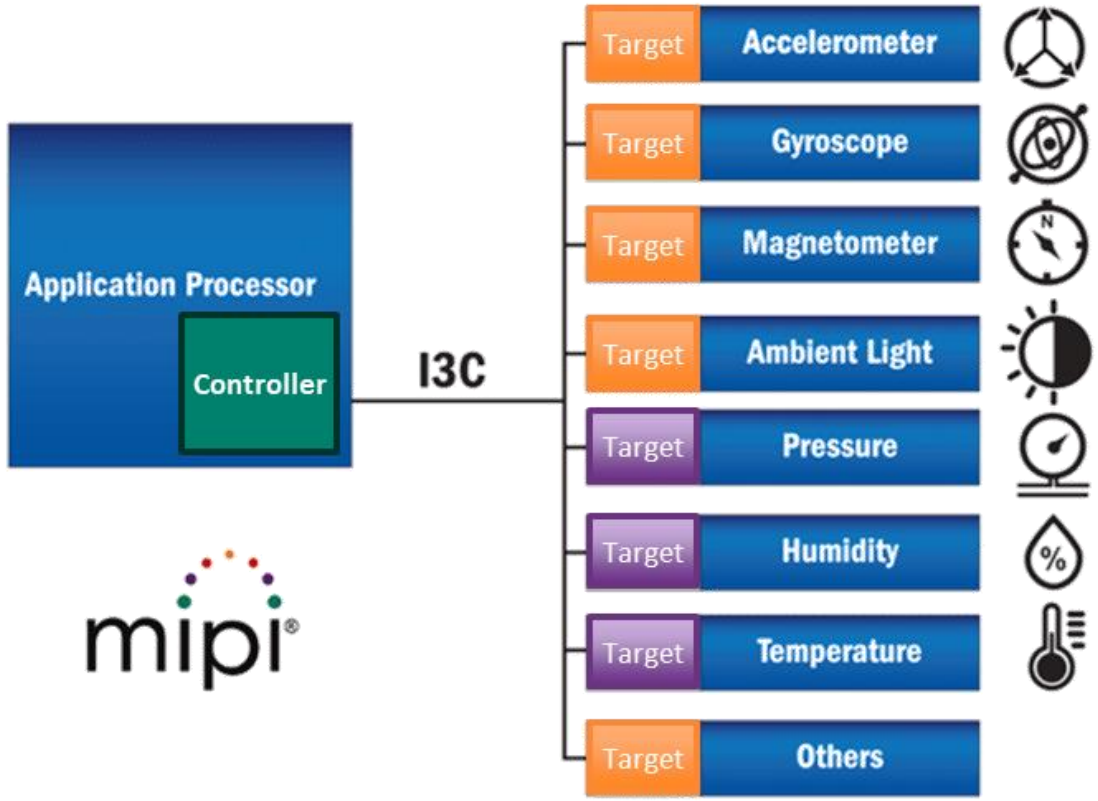


Motivation

- **Urgent need** for a **zero-power subsystem** to power-gate I3C Target & related peripherals.
- The I3C sub-system should handle **remote communication events** (very random & unpredictable).
- **Power duty-cycling** is not efficient.
- Present solutions = **high latency** & **susceptible to data omissions**.

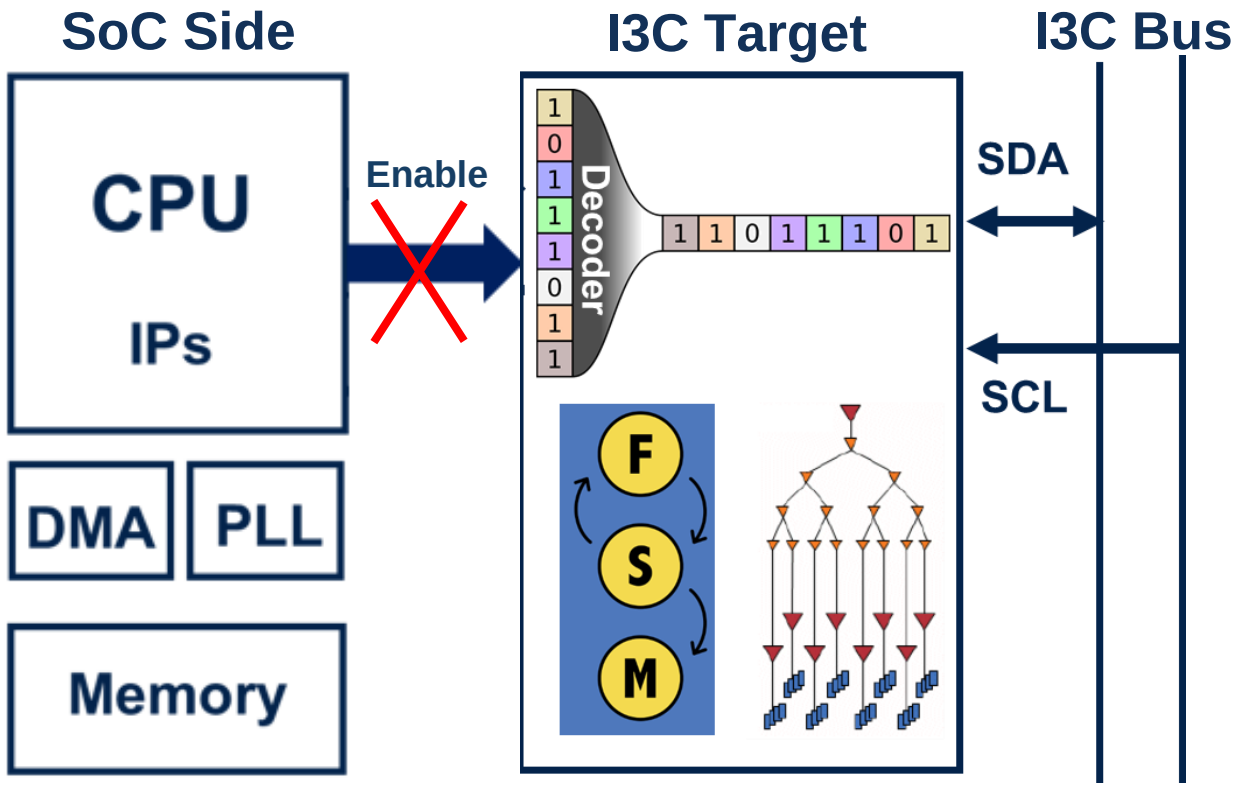


Requirements of low-power IoT



Main Idea

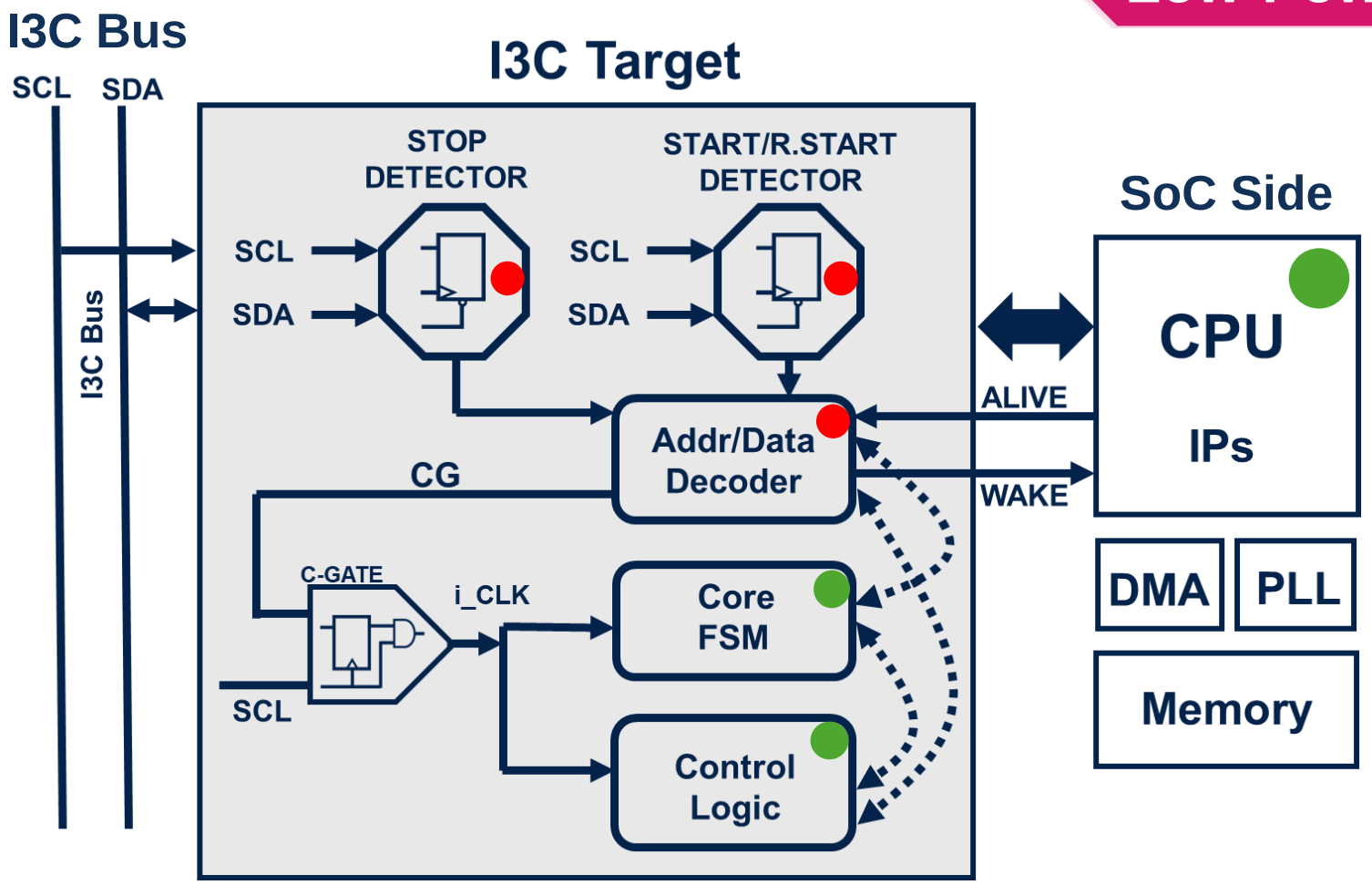
Moving Beyond the Enable Pin



- Get **rid** of the **“Enable”** I3C pin
- CPU/Processor **“Wake up” initiated by I3C Target**
- Wake up done “**Alive**” asserted by CPU
- **No external system clock** for I3C Target
- I3C Target has **self switch-off** mechanism
- FSM, control logic, clock tree mostly static in **low-power mode**

Introducing Smart Partitioning

Low-Power I3C Target

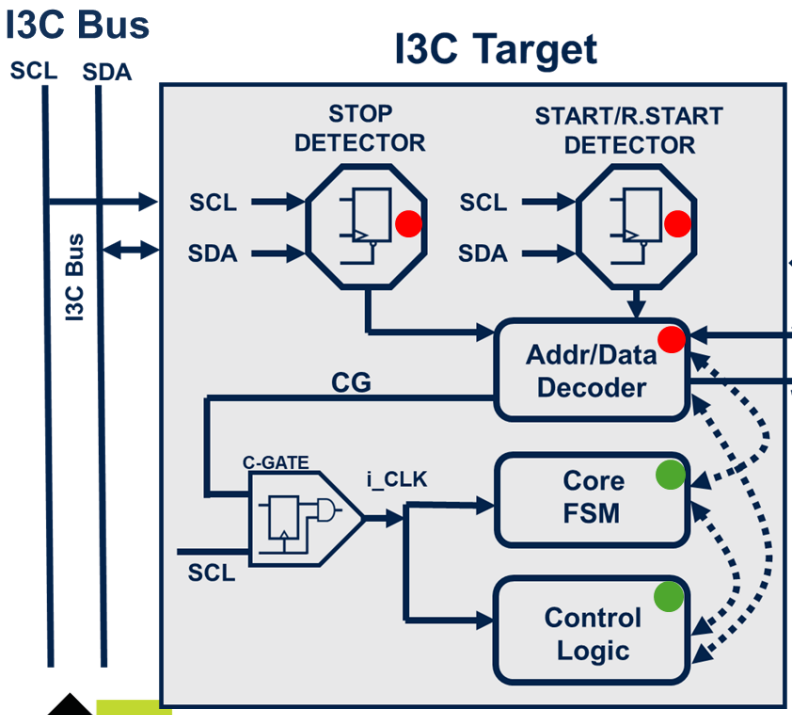


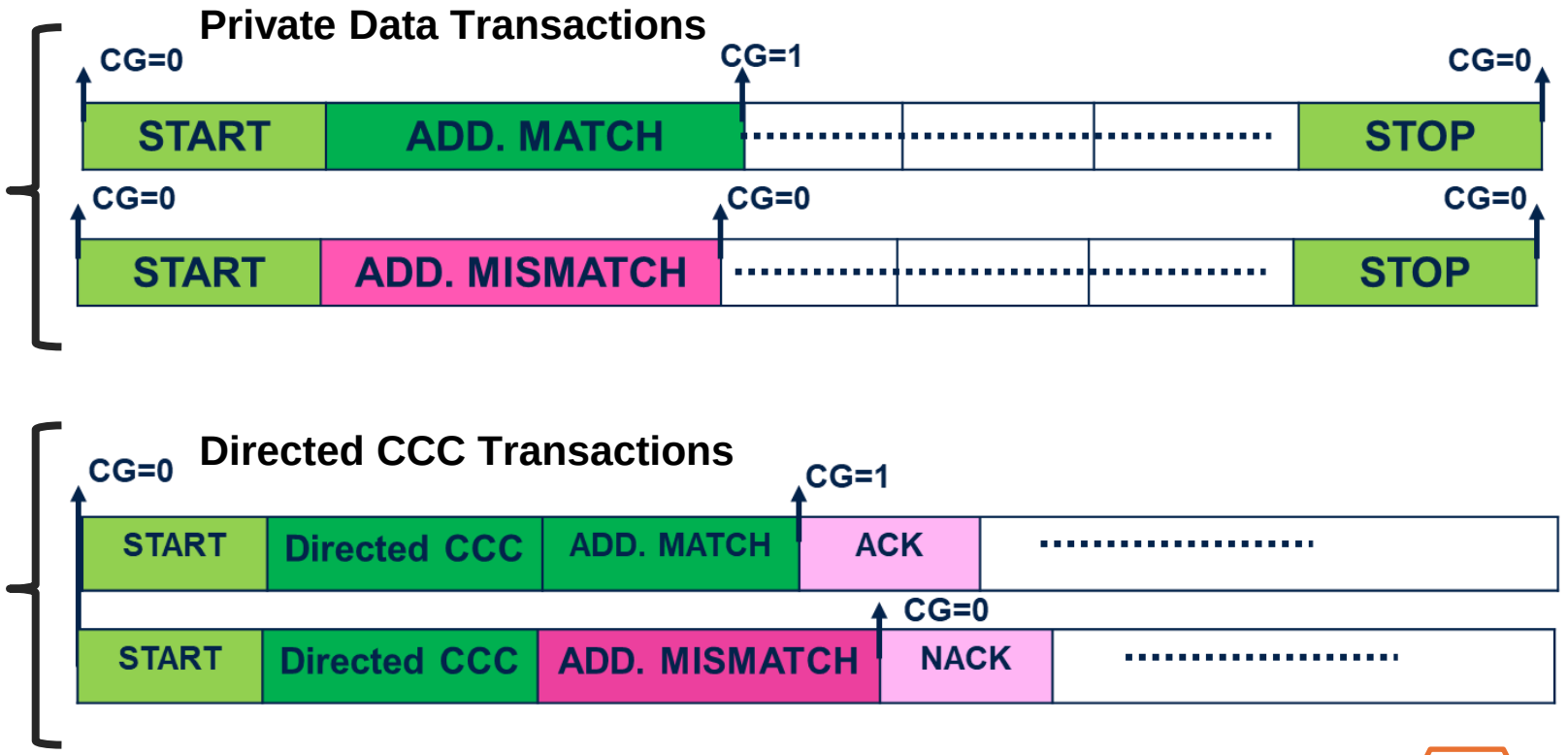
- **Activate** I3C controller components **only on need-to basis.**
- **Powered-up and down** depending on the **relevance of the bus activity** to the system.

Smart Power Management-Address Decoding

Leave the SoC & I3C IP Idle for Unmatched Address !

I3C Target power savings

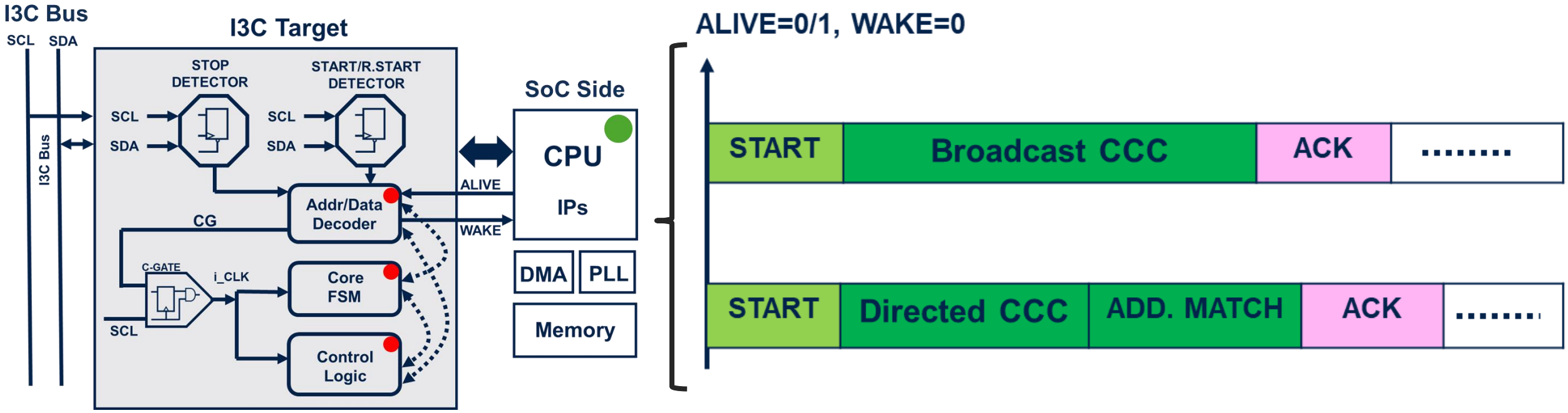




Autonomous Handling of CCC Transactions

CPU Subsystem power savings (1)

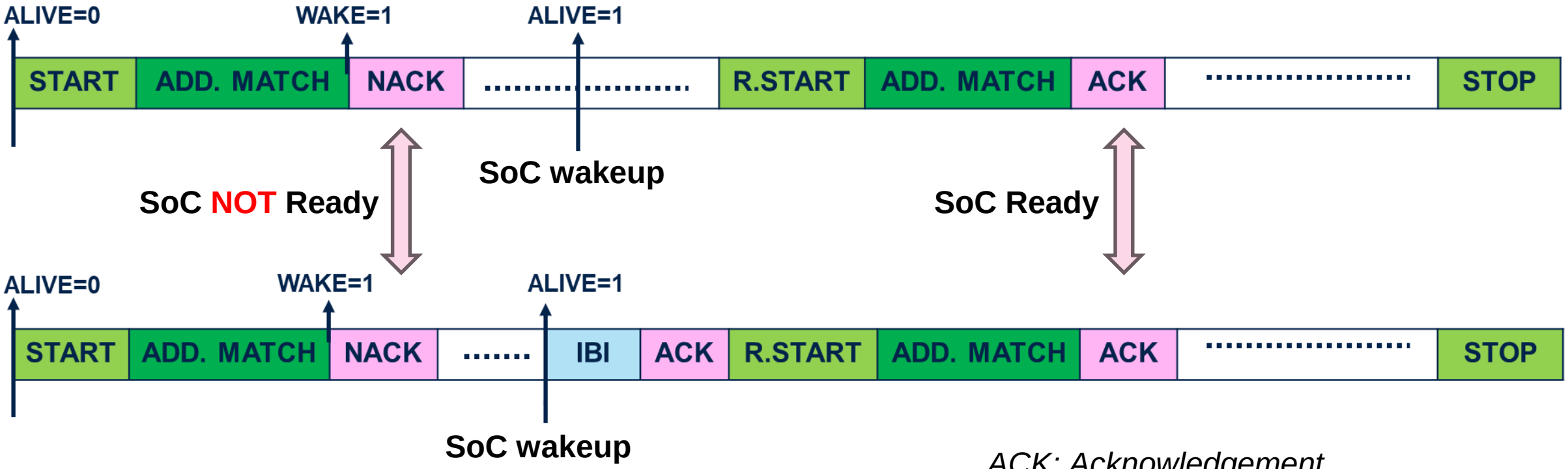
Leave the SoC Idle for CCC Transactions !



Coordinated Wake-Up for Private Transactions

CPU Subsystem power savings (2)

Time to wakes up the SoC for Burst Transactions !



ACK: Acknowledgement
NACK: Not Acknowledgement

Efficiency with Smart Partitioning

Power-up only when essential!

IP intelligently enters low-power mode = Zero latency, No missed transactions
= No unnecessary wake-ups
= Maximum Power Saving

PRIOR APPROACH → **NEW APPROACH**

Enable	IP	SoC
0		
1		

ALIVE	Types of Transactions	ADD.MATCH	WAKE	IP	SoC
0	Broadcast CCC	X	0		
0	Directed CCC	1	0		
0	Private Read/Write	1	1		
1	Full-power mode	0	X		

Takeaways

No interference or customization in I3C global standard protocol

I3C Target IP

- **Zero Wake-up latency**
- **Self initiated Sleep & Wake-up**
- **Removed Enable** control
- **Never isolated** from the I3C Bus
- **Activate only on a need basis**
- Key components mostly in **low-power mode**

I3C subsystem (CPU/Processor)

- **Smart power-on**
- **zero-power subsystem** for I3C Target
- Communicates through **Alive**
- **Enables full I3C** Target functionality
- **No external system clock** for I3C Target
- **Wake-up** initiated **by I3C Target**

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